19-2916; Rev 1; 10/03

EVALUATION KIT AVAILABLE

MAXIM

Ultra-Low-Power, High-Dynamic-Performance, 40Msps Analog Front End

MAX5865

General Description

The MAX5865 ultra-low-power, highly integrated analog front end is ideal for portable communication equipment such as handsets, PDAs, WLAN, and 3G wireless terminals. The MAX5865 integrates dual 8-bit receive ADCs and dual 10-bit transmit DACs while providing the highest dynamic performance at ultra-low power. The ADCs' analog I-Q input amplifiers are fully differential and accept $1V_{P-P}$ full-scale signals. Typical I-Q channel phase matching is ±0.2° and amplitude matching is ±0.05dB. The ADCs feature 48.4dB SINAD and 70dBc spurious-free dynamic range (SFDR) at f_{IN} = 5.5MHz and f_{CLK} = 40MHz. The DACs' analog I-Q outputs are fully differential with ±400mV full-scale output, and 1.4V common-mode level. Typical I-Q channel phase matching is ±0.15° and gain matching is ±0.05dB. The DACs also feature dual 10-bit resolution with 72dBc SFDR, and 57dB SNR at f_{OUT} = 2.2MHz and f_{CLK} = 40MHz.

The ADCs and DACs operate simultaneously or independently for frequency-division duplex (FDD) and time-division duplex (TDD) modes. A 3-wire serial interface controls power-down and transceiver modes of operation. The typical operating power is 75.6mW at f_{CLK} = 40Msps with the ADCs and DACs operating simultaneously in transceiver mode. The MAX5865 features an internal 1.024V voltage reference that is stable over the entire operating power-supply range and temperature range. The MAX5865 operates on a +2.7V to +3.3V analog power supply and a +1.8V to +3.3V digital I/O power supply for logic compatibility. The quiescent current is 8.5mA in idle mode and 1µA in shutdown mode. The MAX5865 is specified for the extended (-40°C to +85°C) temperature range and is available in a 48-pin thin QFN package.

Applications

Narrowband/Wideband CDMA Handsets and PDAs

Fixed/Mobile Broadband Wireless Modems

3G Wireless Terminals

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5865ETM	-40°C to +85°C	48 Thin QFN-EP* (7mm x 7mm)
MAX5865E/D	-40°C to +85°C	Dice**

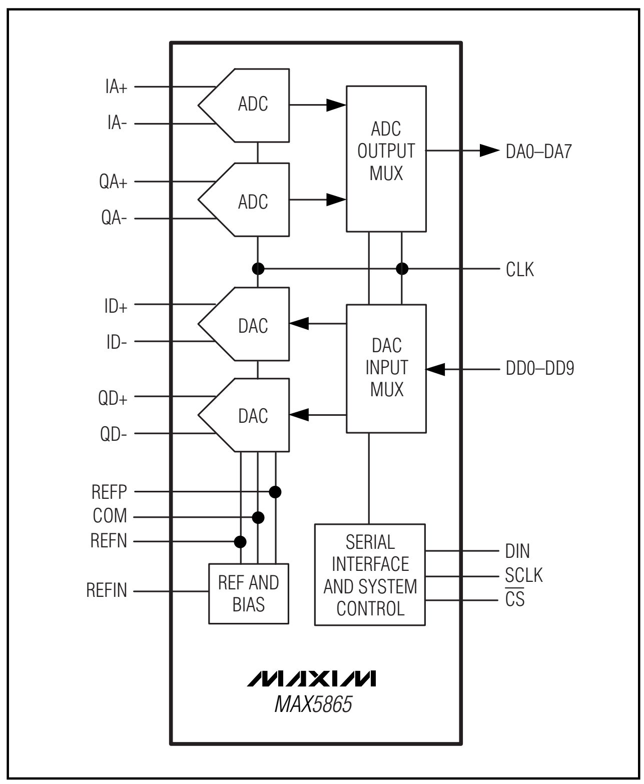
*EP = Exposed paddle.
**Contact factory for dice specifications.

Pin Configuration appears at end of data sheet.

Features

- **Integrated Dual 8-Bit ADCs and Dual 10-Bit DACs**
- **Ultra-Low Power**
  - **75.6mW at f_{CLK} = 40MHz (Transceiver Mode)**
  - **64mW at f_{CLK} = 22MHz (Transceiver Mode)**
  - **Low-Current Idle and Shutdown Modes**
- **Excellent Dynamic Performance**
  - **48.4dB SINAD at f_{IN} = 5.5MHz (ADC)**
  - **70dB SFDR at f_{OUT} = 2.2MHz (DAC)**
- **Excellent Gain/Phase Match**
  - **±0.2° Phase, ±0.05dB Gain at f_{IN} = 5.5MHz (ADC)**
- **Internal/External Reference Option**
- **+1.8V to +3.3V Digital Output Level (TTL/CMOS Compatible)**
- **Multiplexed Parallel Digital Input/Output for ADCs/DACs**
- **Miniature 48-Pin Thin QFN Package (7mm × 7mm)**
- **Evaluation Kit Available (Order MAX5865EVKIT)**

Functional Diagram



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND, OV_{DD} to OGND ....-0.3V to +3.3V
GND to OGND...-0.3V to +0.3V
IA+, IA-, QA+, QA-, ID+, ID-, QD+, QD-, REFP, REFN,
REFIN, COM to GND..............................-0.3V to (V_{DD} + 0.3V)
DD0–DD9, SCLK, DIN, $\overline{CS}$, CLK,
DA0–DA7 to OGND ....-0.3V to (OV_{DD} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
48-Pin Thin QFN (derate 26.3mW/°C above +70°C)..2.1W
Thermal Resistance θ_{JA}...+38°C/W
Operating Temperature Range ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-60°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), C_L ≈ 10pF on all digital outputs, f_{CLK} = 40MHz, ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, Xcvr mode, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS						
Analog Supply Voltage	V_{DD}		2.7	3.0	3.3	V
Output Supply Voltage	OV_{DD}		1.8		V_{DD}	V
V_{DD} Supply Current		ADC operating mode, f_{IN} = 5.5MHz, f_{CLK} = 40MHz, DAC operating mode, f_{OUT} = 2.2MHz		25.2	32	mA
		ADC operating mode (Rx), f_{IN} = 5.5MHz, f_{CLK} = 40MHz, DAC digital inputs at zero or OV_{DD}		21		mA
		DAC operating mode (Tx), f_{OUT} = 2.2MHz, f_{CLK} = 40MHz, ADC off		12.8		mA
		Standby mode, DAC digital inputs and CLK at zero or OV_{DD}			2.0	mA
		Idle mode, DAC digital inputs at zero or OV_{DD}, f_{CLK} = 40MHz			11	mA
		Shutdown mode, digital inputs and CLK at zero or OV_{DD}, $\overline{CS}$ = OV_{DD}		1		µA
OV_{DD} Supply Current		ADC operating mode, f_{IN} = 5.5MHz, f_{CLK} = 40Msps, DAC operating mode, f_{OUT} = 2.2MHz		3.8		mA
		Idle mode, DAC digital inputs at zero or OV_{DD}, f_{CLK} = 40MHz		37.4		µA
		Shutdown mode, DAC digital inputs and CLK at zero or OV_{DD}, $\overline{CS}$ = OV_{DD}		1		µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), C_L ≈ 10pF on all digital outputs, f_{CLK} = 40MHz, ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, Xcvr mode, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC DC ACCURACY						
Resolution			8			Bits
Integral Nonlinearity	INL			±0.15		LSB
Differential Nonlinearity	DNL	No missing codes over temperature		±0.15		LSB
Offset Error		Residual DC offset error		±0.22	±5	%FS
Gain Error		Includes reference error		±0.48	±5	%FS
DC Gain Matching				±0.03	±0.25	dB
Offset Matching				±3		LSB
Gain Temperature Coefficient				±42		ppm/°C
Power-Supply Rejection	PSRR	Offset error (V_{DD} ±5%)		±0.2		LSB
		Gain error (V_{DD} ±5%)		±0.07		
ADC ANALOG INPUT						
Input Differential Range	V_{ID}	Differential or single-ended inputs		±0.512		V
Input Common-Mode Voltage Range				V_{DD} / 2		V
Input Impedance	R_{IN}	Switched capacitor load		120		kΩ
	C_{IN}			5		pF
ADC CONVERSION RATE						
Maximum Clock Frequency	f_{CLK}	(Note 2)			40	MHz
Data Latency		Channel I		5		Clock cycles
		Channel Q		5.5		
ADC DYNAMIC CHARACTERISTICS (Note 3)						
Signal-to-Noise Ratio	SNR	f_{IN} = 5.5MHz	47	48.5		dB
		f_{IN} = 20MHz		48.2		
Signal-to-Noise and Distortion Ratio	SINAD	f_{IN} = 5.5MHz	46.5	48.4		dB
		f_{IN} = 20MHz		48.2		
Spurious-Free Dynamic Range	SFDR	f_{IN} = 5.5MHz	58	70		dBc
		f_{IN} = 20MHz		70		
Third-Harmonic Distortion	HD3	f_{IN} = 5.5MHz		-75.4		dBc
		f_{IN} = 20MHz		-75		
Intermodulation Distortion	IMD	f_1 = 2MHz, -7dBFS; f_2 = 2.01MHz, -7dBFS		-66		dBc
Third-Order Intermodulation Distortion	IM3	f_1 = 2MHz, -7dBFS; f_2 = 2.01MHz, -7dBFS		-70		dBc
Total Harmonic Distortion	THD	f_{IN} = 5.5MHz		-71	-57	dBc
		f_{IN} = 20MHz		-70		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), C_L ≈ 10pF on all digital outputs, f_{CLK} = 40MHz, ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, Xcvr mode, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

Large-Signal Bandwidth	FBW	A_{IN} = -0.5dBFS		440		MHz
Aperture Delay				3.3		ns
Aperture Jitter				2.7		ps_{RMS}
Overdrive Recovery Time		1.5 × full-scale input		2		ns
ADC INTERCHANNEL CHARACTERISTICS						
Crosstalk Rejection		f_{INX} = 5.5MHz at -0.5dBFS, f_{INY} = 0.3MHz at -0.5dBFS (Note 5)		-75		dB
Amplitude Matching		f_{IN} = 5.5MHz at -0.5dBFS (Note 6)		±0.05		dB
Phase Matching		f_{IN} = 5.5MHz at -0.5dBFS (Note 6)		±0.2		Degrees
DAC DC ACCURACY						
Resolution	N		10			Bits
Integral Nonlinearity	INL			±1		LSB
Differential Nonlinearity	DNL	Guaranteed monotonic		±0.5		LSB
Zero-Scale Error		Residual DC offset		±3		LSB
Full-Scale Error		Include reference error	-35		+35	LSB
DAC DYNAMIC PERFORMANCE						
DAC Conversion Rate		(Note 2)			40	Msps
Noise over Nyquist	N_D	f_{OUT} = 2.2MHz, f_{CLK} = 40MHz		-130.6		dBc/Hz
Output-of-Band Noise Power Density	N_O	f_{OUT} = 1.2MHz, f_{CLK} = 22MHz, offset = 10MHz		-130.9		dBc/Hz
Glitch Impulse				10		pVs
Spurious-Free Dynamic Range	SFDR	f_{CLK} = 40MHz, f_{OUT} = 2.2MHz	59	72.3		dBc
		f_{CLK} = 22MHz, f_{OUT} = 200kHz		73.5		
Total Harmonic Distortion (to Nyquist)	THD	f_{CLK} = 40MHz, f_{OUT} = 2.2MHz		-70	-58.5	dB
Signal-to-Noise Ratio (to Nyquist)	SNR	f_{CLK} = 40MHz, f_{OUT} = 2.2MHz		57		dB
DAC INTERCHANNEL CHARACTERISTICS						
DAC-to-DAC Output Isolation		$f_{OUTX, Y}$ = 2.2MHz, $f_{OUTX, Y}$ = 2.0MHz		80		dB
Gain Mismatch Between DAC Outputs		f_{OUT} = 2.2MHz, f_{CLK} = 40MHz		0.05		dB
Phase Mismatch Between DAC Outputs		f_{OUT} = 2.2MHz, f_{CLK} = 40MHz		±0.15		Degrees

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), C_L ≈ 10pF on all digital outputs, f_{CLK} = 40MHz, ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, Xcvr mode, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DAC ANALOG OUTPUT						
Full-Scale Output Voltage	V_{FS}			±400		mV
Output Common-Mode Range			1.29		1. 5	V
ADC-DAC INTERCHANNEL CHARACTERISTICS						
ADC-DAC Isolation		ADC f_{INI} = f_{INQ} = 5.5MHz, DAC f_{OUTI} = f_{OUTQ} = 2.2MHz, f_{CLK} = 40MHz		75		dB
ADC-DAC TIMING CHARACTERISTICS						
CLK Rise to I-ADC Channel-I Output Data Valid	t_{DOI}	Figure 3 (Note 4)		7.4	9	ns
CLK Fall to Q-ADC Channel-Q Output Data Valid	t_{DOQ}	Figure 3 (Note 4)		6.9	9	ns
I-DAC Data to CLK Fall Setup Time	t_{DSI}	Figure 4 (Note 4)	10			ns
Q-DAC Data to CLK Rise Setup Time	t_{DSQ}	Figure 4 (Note 4)	10			ns
CLK Fall to I-DAC Data Hold Time	t_{DHI}	Figure 4 (Note 4)	0			ns
CLK Rise to Q-DAC Data Hold Time	t_{DHQ}	Figure 4 (Note 4)	0			ns
Clock Duty Cycle				50		%
CLK Duty-Cycle Variation				±15		%
Digital Output Rise/Fall Time		20% to 80%		2.6		ns
SERIAL INTERFACE TIMING CHARACTERISTICS						
Falling Edge of $\overline{CS}$ to Rising Edge of First SCLK Time	t_{CSS}	Figure 5 (Note 4)	10			ns
DIN to SCLK Setup Time	t_{DS}	Figure 5 (Note 4)	10			ns
DIN to SCLK Hold Time	t_{DH}	Figure 5 (Note 4)	0			ns
SCLK Pulse Width High	t_{CH}	Figure 5 (Note 4)	25			ns
SCLK Pulse Width Low	t_{CL}	Figure 5 (Note 4)	25			ns
SCLK Period	t_{CP}	Figure 5 (Note 4)	50			ns
SCLK to $\overline{CS}$ Setup Time	t_{CS}	Figure 5 (Note 4)	0			ns
$\overline{CS}$ High Pulse Width	t_{CSW}	Figure 5 (Note 4)	80			ns
MODE RECOVERY TIMING CHARACTERISTICS						
Shutdown Wake-Up Time	$t_{WAKE,SD}$	From shutdown to Rx mode, Figure 6, ADC settles to within 1dB		20		µs
		From shutdown to Tx mode, Figure 6, DAC settles to within 10 LSB error		40		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), C_L ≈ 10pF on all digital outputs, f_{CLK} = 40MHz, ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, Xcvr mode, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Idle Wake-Up Time (with CLK)	$t_{WAKE,ST0}$	From idle to Rx mode with CLK present during idle, Figure 6, ADC settles to within 1dB SINAD		10		µs
		From idle to Tx mode with CLK present during idle, Figure 6, DAC settles to 10 LSB error		10		
Standby Wake-Up Time	$t_{WAKE,ST1}$	From standby to Rx mode, Figure 6, ADC settles to within 1dB SINAD		10		µs
		From standby to Tx mode, Figure 6, DAC settles to 10 LSB error		40		
Enable Time from Xcvr or Tx to Rx	$t_{ENABLE, Rx}$	ADC settles to within 1dB SINAD		10		µs
Enable Time from Xcvr or Rx to Tx	$t_{ENABLE, Tx}$	DAC settles to 10 LSB error		10		µs
INTERNAL REFERENCE (REFIN = V_{DD}. V_{REFP}, V_{REFN} and V_{COM} are generated internally.)						
Positive Reference		V_{REFP} - V_{COM}		0.256		V
Negative Reference		V_{REFN} - V_{COM}		-0.256		V
Common-Mode Output Voltage	V_{COM}		V_{DD} / 2 - 0.15	V_{DD} / 2	V_{DD} / 2 + 0.15	V
Differential Reference Output	V_{REF}	V_{REFP} - V_{REFN}	+0.49	+0.512	+0.534	V
Differential Reference Temperature Coefficient	REFTC			±30		ppm/°C
Maximum REFP/REFN/COM Source Current	I_{SOURCE}			2		mA
Maximum REFP/REFN/COM Sink Current	I_{SINK}			2		mA
BUFFERED EXTERNAL REFERENCE (REFIN = 1.024V. V_{REFP}, V_{REFN}, and V_{COM} are generated internally.)						
Reference Input	V_{REFIN}			1.024		V
Differential Reference Output	V_{DIFF}	V_{REFP} - V_{REFN}		0.512		V
Common-Mode Output Voltage	V_{COM}			V_{DD} / 2		V
Maximum REFP/REFN/COM Source Current	I_{SOURCE}			2		mA
Maximum REFP/REFN/COM Sink Current	I_{SINK}			2		mA
REFIN Input Resistance				>500		kΩ
REFIN Input Current				-0.7		µA
DIGITAL INPUTS (CLK, SCLK, DIN, $\overline{CS}$, DD0–DD9)						
Input High Threshold	V_{INH}	DD0–DD9, CLK, SCLK, DIN, $\overline{CS}$	0.7 x OV_{DD}			V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), C_L ≈ 10pF on all digital outputs, f_{CLK} = 40MHz, ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, Xcvr mode, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Threshold	V_{INL}	DD0–DD9, CLK, SCLK, DIN, $\overline{CS}$			0.3 x OV_{DD}	V
Input Leakage	DI_{IN}	DD0–DD9, CLK, SCLK, DIN, $\overline{CS}$ = OGND or OV_{DD}			±5	µA
Input Capacitance	DC_{IN}			5		pF
DIGITAL OUTPUTS (DA0–DA7)						
Output Voltage Low	V_{OL}	I_{SINK} = 200µA			0.2 x OV_{DD}	V
Output Voltage High	V_{OH}	I_{SOURCE} = 200µA	0.8 x OV_{DD}			V
Tri-State Leakage Current	I_{LEAK}				±5	µA
Tri-State Output Capacitance	C_{OUT}			5		pF

Note 1: Specifications from T_A = +25°C to +85°C are guaranteed by product tests. Specifications from T_A = +25°C to -40°C are guaranteed by design and characterization.

Note 2: The minimum clock frequency for the MAX5865 is 22MHz.

Note 3: SNR, SINAD, SFDR, HD3, and THD are based on a differential analog input voltage of -0.5dBFS referenced to the amplitude of the digital outputs. SINAD and THD are calculated using HD2 through HD6.

Note 4: Guaranteed by design and characterization.

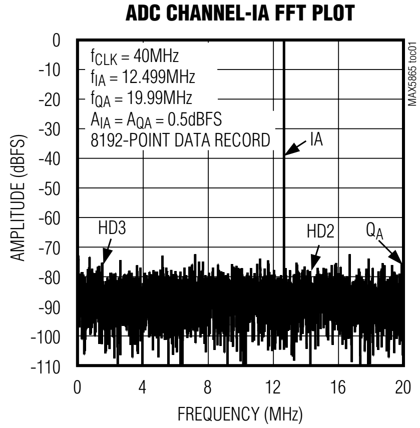
Note 5: Crosstalk rejection is measured by applying a high-frequency test tone to one channel and a low-frequency tone to the second channel. FFTs are performed on each channel. The parameter is specified as the power ratio of the first and second channel FFT test tone bins.

Note 6: Amplitude/phase matching is measured by applying the same signal to each channel, and comparing the magnitude and phase of the fundamental bin on the calculated FFT.

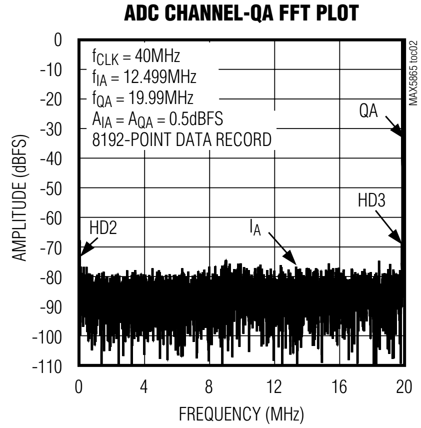
Typical Operating Characteristics

(V_{DD} = DV_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), C_L ≈ 10pF on all digital outputs, f_{CLK} = 40MHz 50% duty cycle, ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, Xcvr mode, T_A = +25°C, unless otherwise noted.)

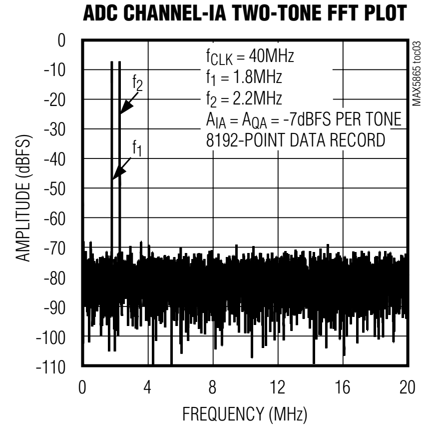
ADC CHANNEL-IA FFT PLOT



ADC CHANNEL-QA FFT PLOT



ADC CHANNEL-IA TWO-TONE FFT PLOT

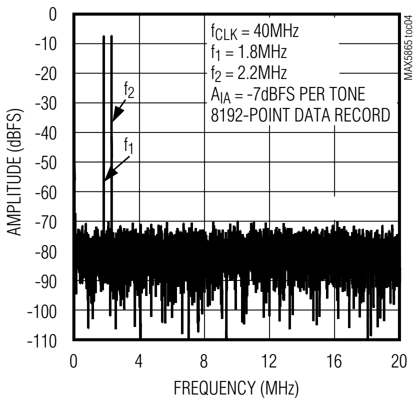


Ultra-Low-Power, High-Dynamic-Performance, 40Msps Analog Front End

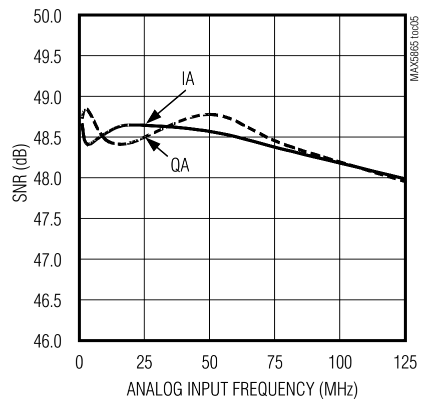
Typical Operating Characteristics (continued)

(V_{DD} = DV_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), C_L ≈ 10pF on all digital outputs, f_{CLK} = 40MHz 50% duty cycle, ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, Xcvr mode, T_A = +25°C, unless otherwise noted.)

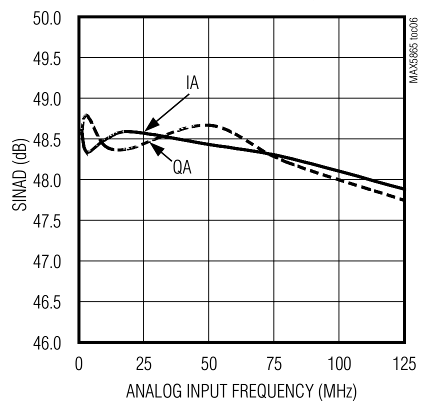
ADC CHANNEL-QA TWO-TONE FFT PLOT



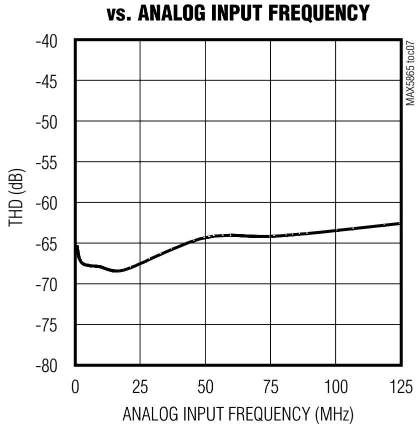
ADC SIGNAL-TO-NOISE RATIO vs. ANALOG INPUT FREQUENCY



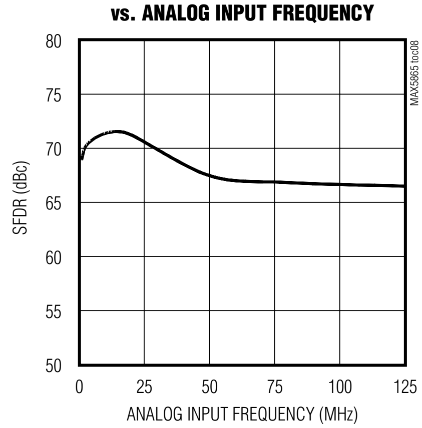
ADC SIGNAL-TO-NOISE AND DISTORTION RATIO vs. ANALOG INPUT FREQUENCY



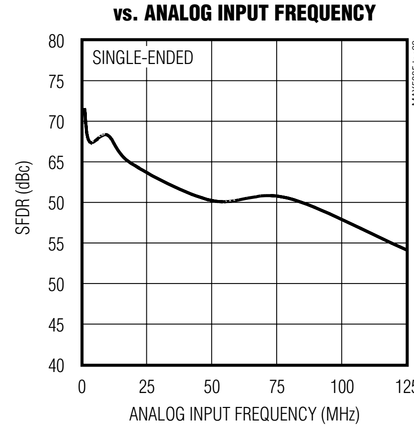
ADC TOTAL HARMONIC DISTORTION vs. ANALOG INPUT FREQUENCY



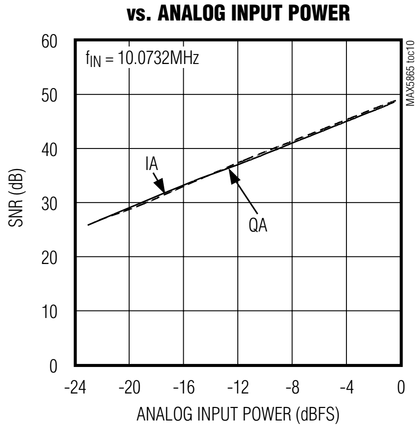
ADC SPURIOUS-FREE DYNAMIC RANGE vs. ANALOG INPUT FREQUENCY



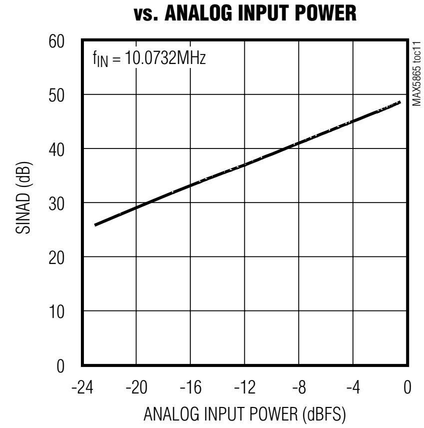
ADC SPURIOUS-FREE DYNAMIC RANGE vs. ANALOG INPUT FREQUENCY



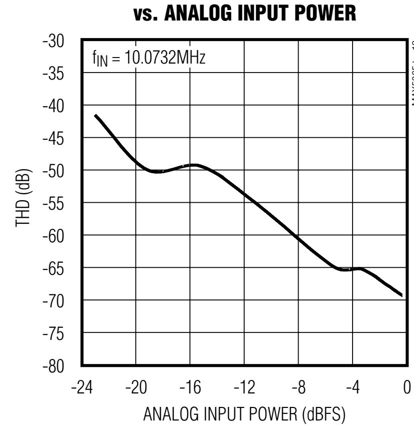
ADC SIGNAL-TO-NOISE RATIO vs. ANALOG INPUT POWER



ADC SIGNAL-TO-NOISE AND DISTORTION RATIO vs. ANALOG INPUT POWER



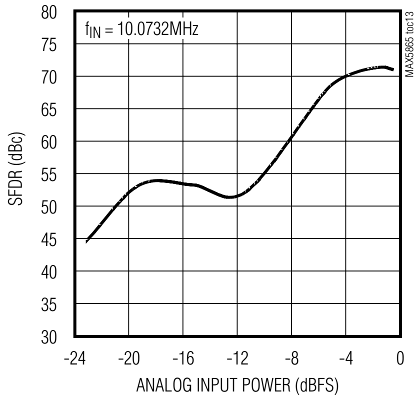
ADC TOTAL HARMONIC DISTORTION vs. ANALOG INPUT POWER



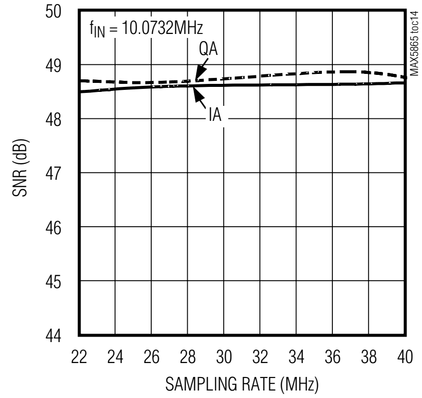
Typical Operating Characteristics (continued)

(V_{DD} = DV_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), C_L ≈ 10pF on all digital outputs, f_{CLK} = 40MHz 50% duty cycle, ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, Xcvr mode, T_A = +25°C, unless otherwise noted.)

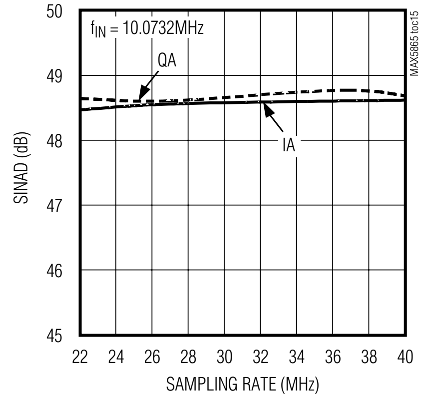
ADC SPURIOUS-FREE DYNAMIC RANGE vs. ANALOG INPUT POWER



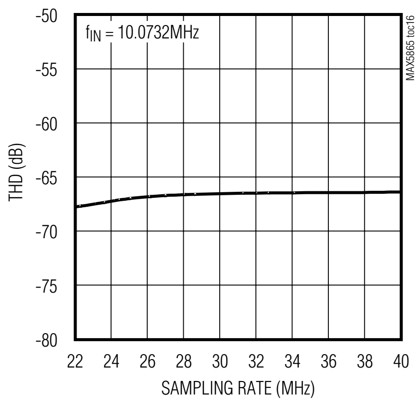
ADC SIGNAL-TO-NOISE RATIO vs. SAMPLING RATE



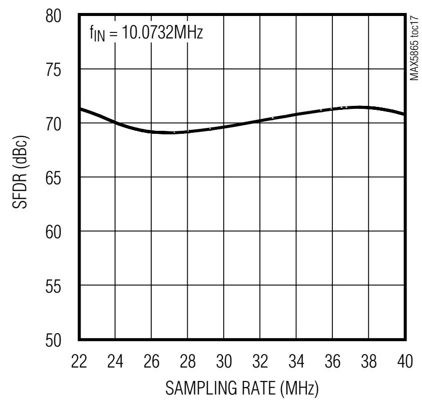
ADC SIGNAL-TO-NOISE AND DISTORTION RATIO vs. SAMPLING RATE



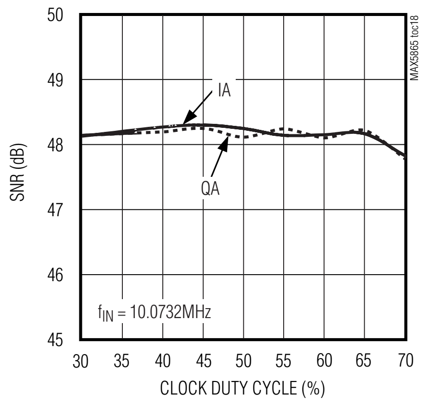
ADC TOTAL HARMONIC DISTORTION vs. SAMPLING RATE



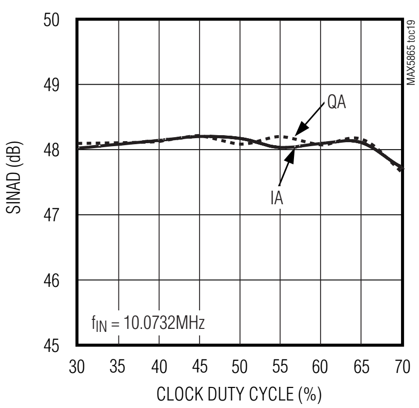
ADC SPURIOUS-FREE DYNAMIC RANGE vs. SAMPLING RATE



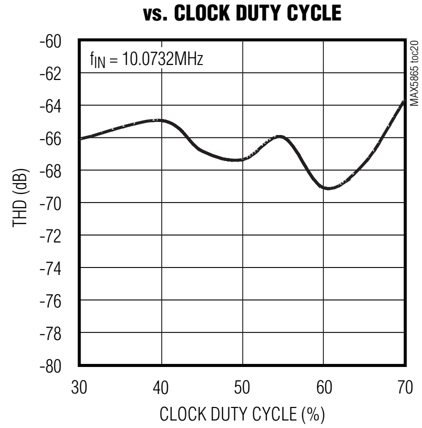
ADC SIGNAL-TO-NOISE RATIO vs. CLOCK DUTY CYCLE



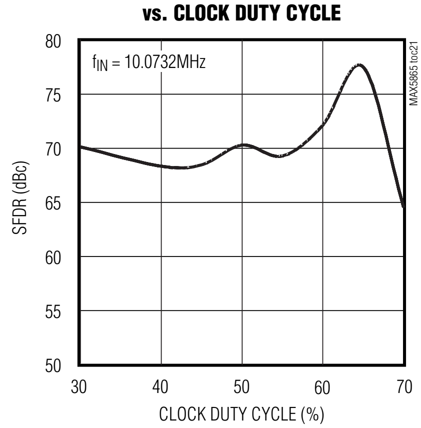
ADC SIGNAL-TO-NOISE AND DISTORTION RATIO vs. CLOCK DUTY CYCLE



ADC TOTAL HARMONIC DISTORTION vs. CLOCK DUTY CYCLE



ADC SPURIOUS-FREE DYNAMIC RANGE vs. CLOCK DUTY CYCLE

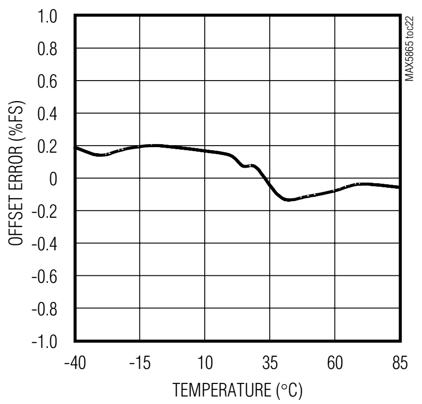


Ultra-Low-Power, High-Dynamic-Performance, 40Msps Analog Front End

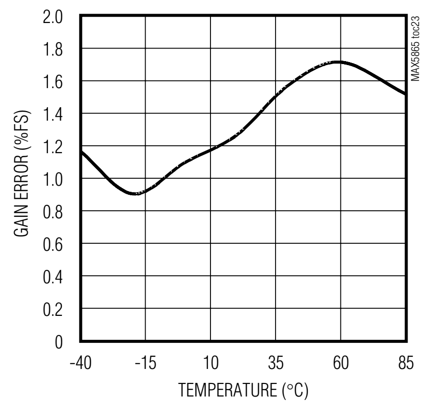
Typical Operating Characteristics (continued)

(V_{DD} = DV_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), C_L ≈ 10pF on all digital outputs, f_{CLK} = 40MHz 50% duty cycle, ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, Xcvr mode, T_A = +25°C, unless otherwise noted.)

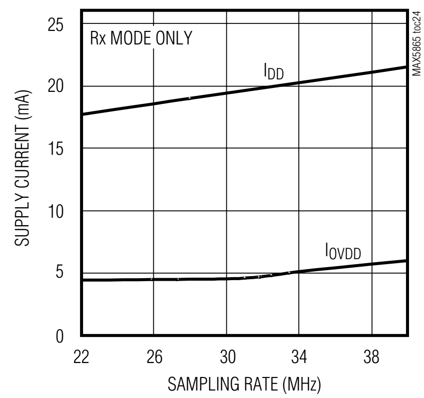
ADC OFFSET ERROR vs. TEMPERATURE



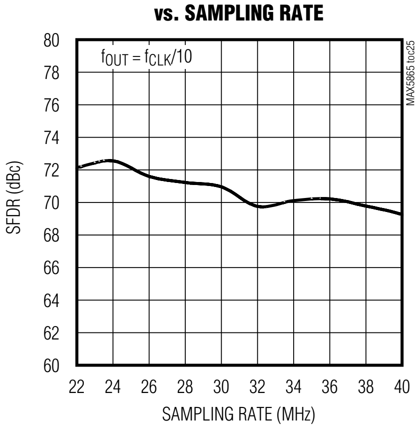
ADC GAIN ERROR vs. TEMPERATURE



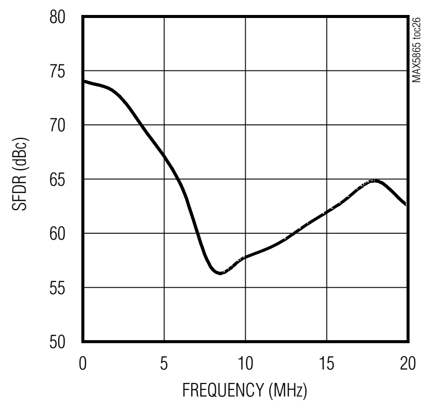
SUPPLY CURRENT vs. SAMPLING RATE



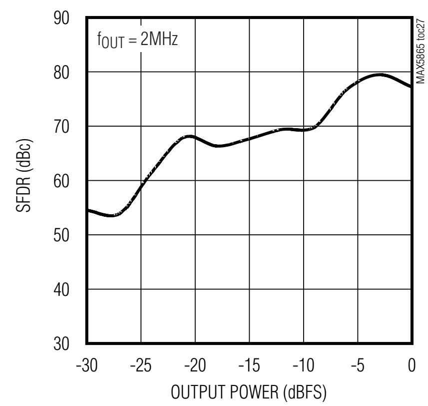
DAC SPURIOUS-FREE DYNAMIC RANGE vs. SAMPLING RATE



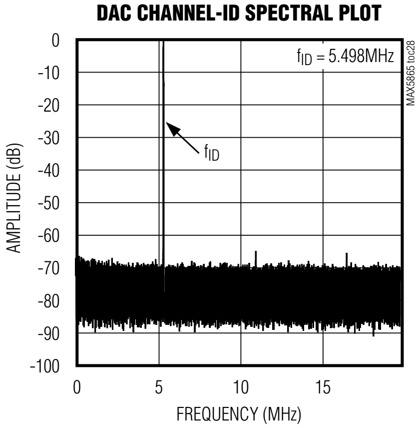
DAC SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY



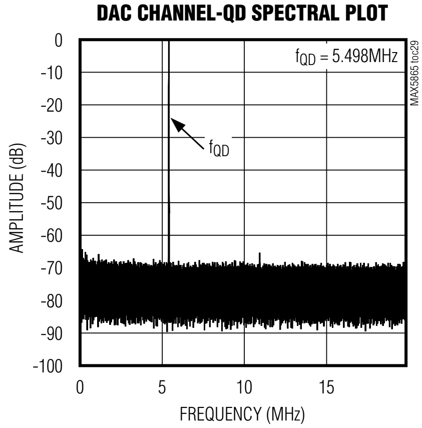
DAC SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT POWER



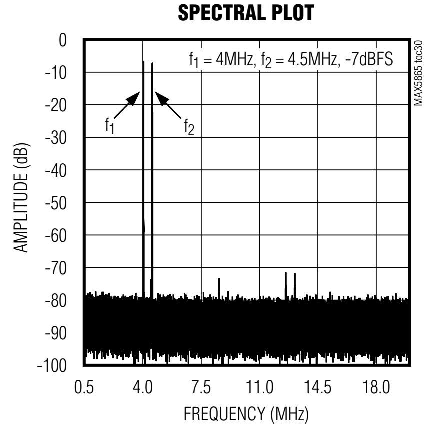
DAC CHANNEL-ID SPECTRAL PLOT



DAC CHANNEL-QD SPECTRAL PLOT

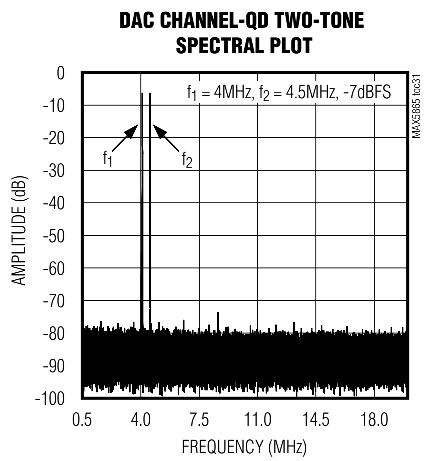


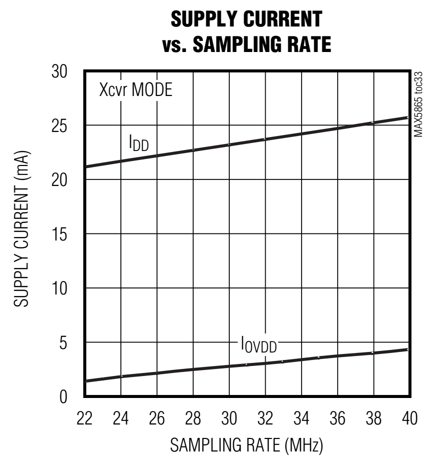
DAC CHANNEL-ID TWO-TONE SPECTRAL PLOT

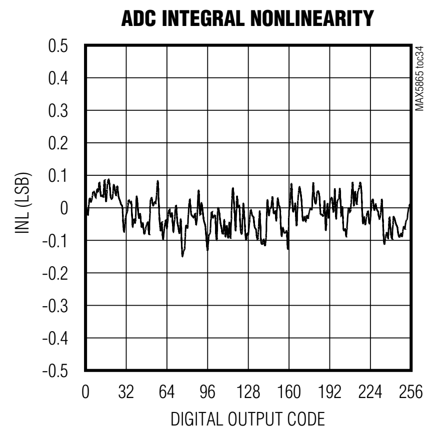


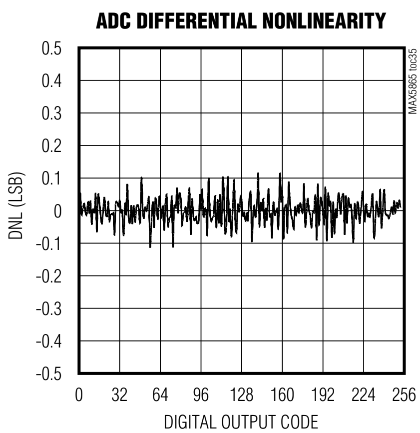
Typical Operating Characteristics (continued)

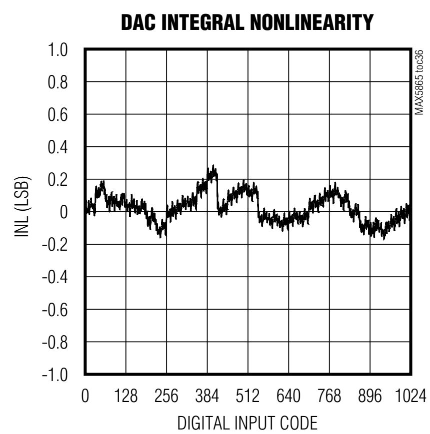
(V_{DD} = DV_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), C_L ≈ 10pF on all digital outputs, f_{CLK} = 40MHz 50% duty cycle, ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, Xcvr mode, T_A = +25°C, unless otherwise noted.)

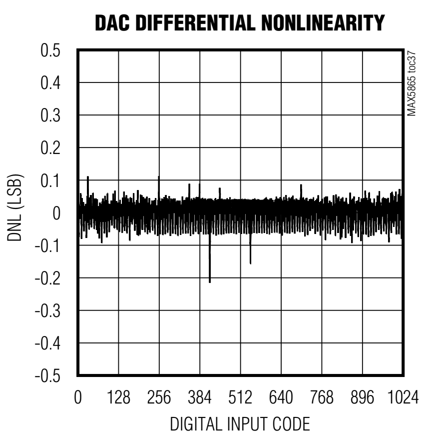


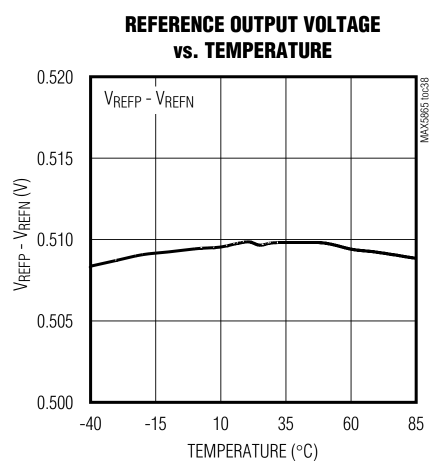












Ultra-Low-Power, High-Dynamic-Performance, 40Msps Analog Front End

Pin Description

PIN	NAME	FUNCTION
1	REFP	Upper Reference Voltage. Bypass with a 0.33µF capacitor to GND as close to REFP as possible.
2, 8, 43	V_{DD}	Analog Supply Voltage. Bypass V_{DD} to GND with a combination of a 2.2µF capacitor in parallel with a 0.1µF capacitor.
3	IA+	Channel IA Positive Analog Input. For single-ended operation, connect signal source to IA+.
4	IA-	Channel IA Negative Analog Input. For single-ended operation, connect IA- to COM.
5, 7, 12, 37, 42	GND	Analog Ground. Connect all pins to GND ground plane.
6	CLK	Conversion Clock Input. Clock signal for both ADCs and DACs.
9	QA-	Channel QA Negative Analog Input. For single-ended operation, connect QA- to COM.
10	QA+	Channel QA Positive Analog Input. For single-ended operation, connect signal source to QA+.
11, 33, 39	V_{DD}	Analog Supply Voltage. Connect to V_{DD} power plane as close to the device as possible.
13–16, 19–22	DA0–DA7	ADC Tri-State Digital Output Bits. DA7 is the most significant bit (MSB), and DA0 is the least significant bit (LSB).
17	OGND	Output Driver Ground
18	OV_{DD}	Output Driver Power Supply. Supply range from +1.8V to V_{DD} to accommodate most logic levels. Bypass OV_{DD} to OGND with a combination of a 2.2µF capacitor in parallel with a 0.1µF capacitor.
23–32	DD0–DD9	DAC Digital Input Bits. DD9 is the MSB, and DD0 is the LSB.
34	DIN	3-Wire Serial Interface Data Input. Data is latched on the rising edge of the SCLK.
35	SCLK	3-Wire Serial Interface Clock Input
36	$\overline{CS}$	3-Wire Serial Interface Chip Select Input. Apply logic low enables the serial interface.
38	N.C.	No Connection
40, 41	QD+, QD-	DAC Channel-QD Differential Voltage Output
44, 45	ID-, ID+	DAC Channel-ID Differential Voltage Output
46	REFIN	Reference Input. Connect to V_{DD} for internal reference.
47	COM	Common-Mode Voltage I/O. Bypass COM to GND with a 0.33µF capacitor.
48	REFN	Negative Reference I/O. Conversion range is $\pm(V_{REFP} - V_{REFN})$. Bypass REFN to GND with a 0.33µF capacitor.
—	EP	Exposed Paddle. Exposed paddle is internally connected to GND. Connect EP to the GND plane.

Detailed Description

The MAX5865 integrates dual 8-bit receive ADCs and dual 10-bit transmit DACs while providing ultra-low power and highest dynamic performance at a conversion rate of 40Msps. The ADCs' analog input amplifiers are fully differential and accept $1V_{P-P}$ full-scale signals. The DACs' analog outputs are fully differential with ±400mV full-scale output range at 1.4V common mode.

The MAX5865 includes a 3-wire serial interface to control operating modes and power management. The serial interface is SPI™ and MICROWIRE™ compatible. The MAX5865 serial interface selects shutdown, idle, standby, transmit, receive, and transceiver modes.

The MAX5865 can operate in FDD or TDD applications by configuring the device for transmit, receive, or transceiver modes through a 3-wire serial interface. In TDD mode, the digital bus for receive ADC and transmit DAC can be shared to reduce the digital I/O to a single 10-bit parallel multiplexed bus. In FDD mode, the MAX5865 digital I/O can be configured for an 18-bit, parallel multiplexed bus to match the dual 8-bit ADC and dual 10-bit DAC.

The MAX5865 features an internal precision 1.024V bandgap reference that is stable over the entire power-supply and temperature ranges.

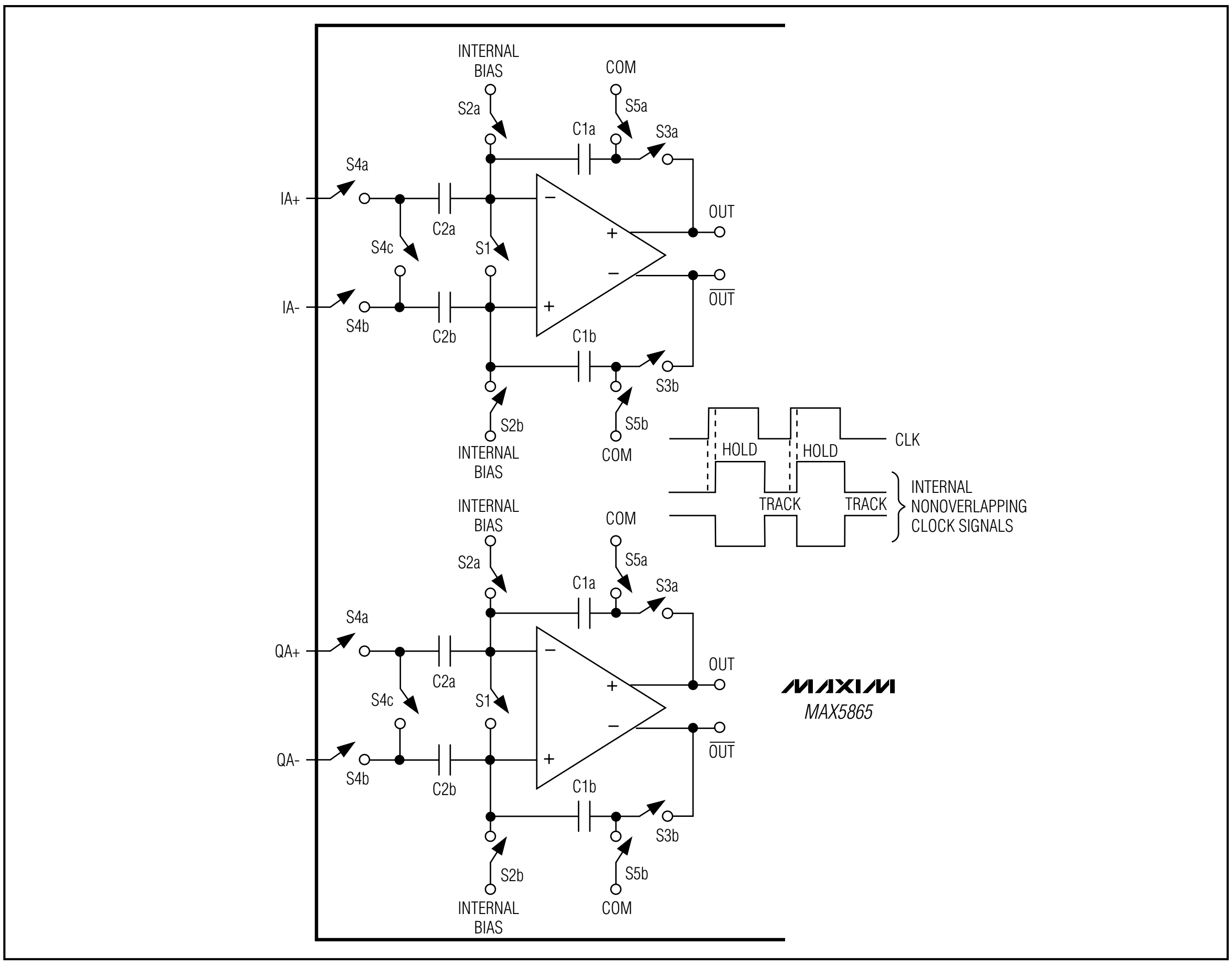


Figure 1. MAX5865 ADC Internal T/H Circuits

SPI is a trademark of Motorola, Inc. MICROWIRE is a trademark of National Semiconductor Corp.

Ultra-Low-Power, High-Dynamic-Performance, 40Msps Analog Front End

Dual 8-Bit ADC

The ADC uses a seven-stage, fully differential, pipelined architecture that allows for high-speed conversion while minimizing power consumption. Samples taken at the inputs move progressively through the pipeline stages every half-clock cycle. Including the delay through the output latch, the total clock-cycle latency is 5 clock cycles for channel IA and 5.5 clock cycles for channel QA. The ADC's full-scale analog input range is $\pm V_{REF}$ with a common-mode input range of $V_{DD}/2$ ±0.2V. V_{REF} is the difference between V_{REFP} and V_{REFN}. See the *Reference Configurations* section for details.

Input Track-and-Hold (T/H) Circuits

Figure 1 displays a simplified functional diagram of the ADC's input T/H circuitry. In track mode, switches S1, S2a, S2b, S4a, S4b, S5a, and S5b are closed. The fully differential circuits sample the input signals onto the two capacitors (C2a and C2b) through switches S4a and S4b. S2a and S2b set the common mode for the amplifier input, and open simultaneously with S1, sampling the input waveform. Switches S4a, S4b, S5a, and S5b are then opened before switches S3a and S3b connect capacitors C1a and C1b to the output of the amplifier and switch S4c is closed. The resulting differential voltages are held on capacitors C2a and C2b. The amplifiers charge capacitors C1a and C1b to the same values originally held on C2a and C2b. These values are then presented to the first-stage quantizers and isolate the pipelines from the fast-changing inputs. The wide input bandwidth T/H amplifiers allow the ADC to track and sample/hold analog inputs of high frequencies (> Nyquist). Both ADC inputs (IA+, QA+, IA-, and QA-) can be driven either differentially or single ended. Match the impedance of IA+ and IA-, as well as QA+ and QA-, and set the common-mode voltage to mid-supply ($V_{DD}/2$) for optimum performance.

ADC Digital Output Data (DA0–DA7)

DA0–DA7 are the ADCs' digital logic outputs. The logic level is set by OV_{DD} from 1.8V to V_{DD}. The digital output coding is offset binary (Table 1, Figure 2). The capacitive load on digital outputs DA0–DA7 should be kept as low as possible (<15pF) to avoid large digital currents feeding back into the analog portion of the MAX5865 and degrading its dynamic performance. Buffers on the digital outputs isolate them from heavy capacitive loads. Adding 100Ω resistors in series with the digital outputs close to the MAX5865 helps improve ADC performance. Refer to the MAX5865 EV kit schematic for an example of the digital outputs driving a digital buffer through 100Ω series resistors.

Table 1. Output Codes vs. Input Voltage

DIFFERENTIAL INPUT VOLTAGE	DIFFERENTIAL INPUT (LSB)	OFFSET BINARY (DA7–DA0)	OUTPUT DECIMAL CODE
$V_{REF} \times \frac{127}{128}$	127 (+full scale - 1LSB)	1111 1111	255
$V_{REF} \times \frac{126}{128}$	126 (+full scale - 2LSB)	1111 1110	254
$V_{REF} \times \frac{1}{128}$	+1	1000 0001	129
$V_{REF} \times \frac{0}{128}$	0 (bipolar zero)	1000 0000	128
$-V_{REF} \times \frac{1}{128}$	-1	0111 1111	127
$-V_{REF} \times \frac{127}{128}$	-127 (-full scale + 1LSB)	0000 0001	1
$-V_{REF} \times \frac{128}{128}$	-128 (-full scale)	0000 0000	0

ADC System Timing Requirements

Figure 3 shows the relationship between the clock, analog inputs, and the resulting output data. Channel IA (CHI) and channel QA (CHQ) are simultaneously sampled on the rising edge of the clock signal (CLK) and the resulting data is multiplexed at the DA0–DA7 outputs. CHI data is updated on the rising edge and CHQ data is updated on the falling edge of the CLK. Including the delay through the output latch, the total clock-cycle latency is 5 clock cycles for CHI and 5.5 clock cycles for CHQ.

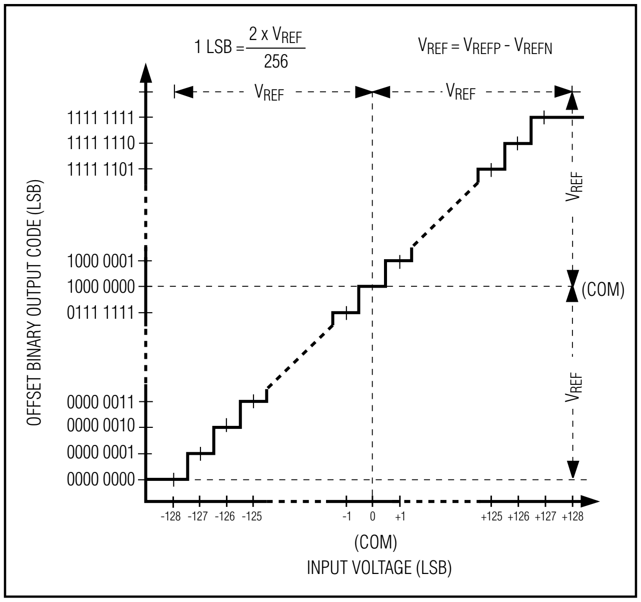


Figure 2. ADC Transfer Function

Dual 10-Bit DAC

The 10-bit DACs are capable of operating with clock speeds up to 40MHz. The DAC's digital inputs, DD0–DD9, are multiplexed on a single 10-bit bus. The voltage reference determines the data converters' full-scale output voltages. See the *Reference Configurations* section for setting reference voltage. The DACs utilize a current-array technique with a 1mA (with 1.024V reference) full-scale output current driving a 400Ω internal resistor resulting in a ±400mV full-scale differential output voltage. The MAX5865 is designed for differential output only and is not intended for single-ended application. The analog outputs are biased at 1.4V common mode and designed to drive a differential input stage with input impedance ≥70kΩ. This simplifies the analog interface between RF quadrature upconverters and the MAX5865. RF upconverters require a 1.3V to 1.5V common-mode bias. The internal DC common-mode bias eliminates discrete level setting resistors and code-generated level-shifting while preserving the full dynamic range of each transmit DAC. Table 2 shows the output voltage vs. input code.

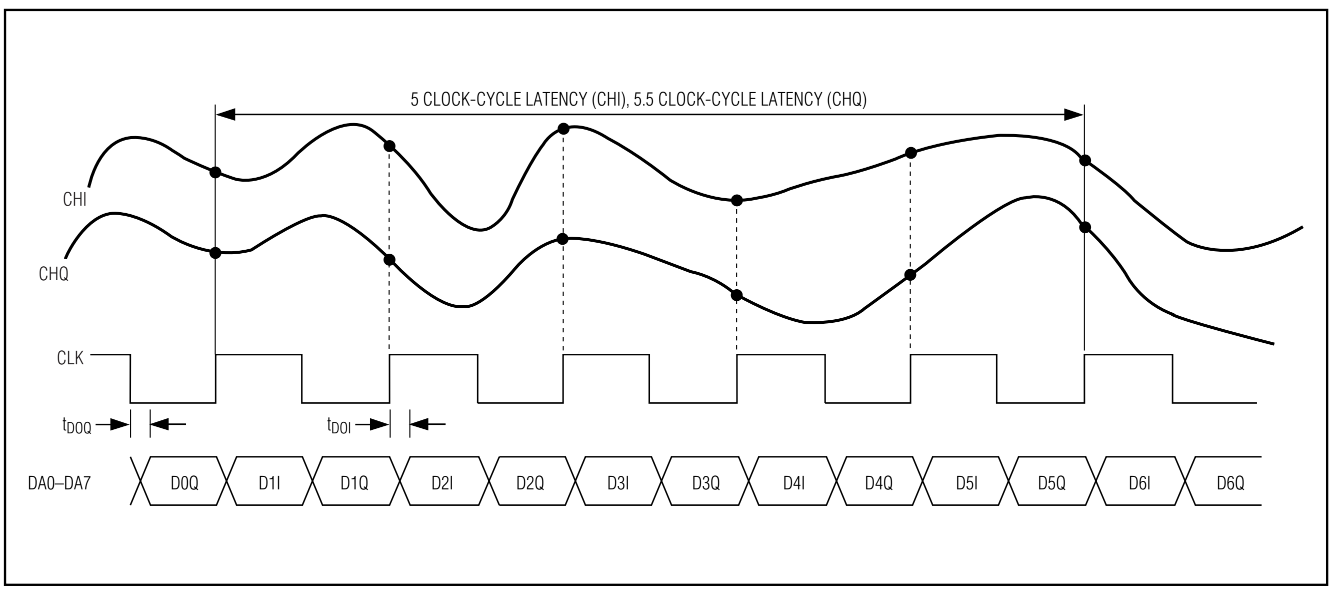


Figure 3. ADC System Timing Diagram

Table 2. DAC Output Voltage vs. Input Codes (Internal Reference Mode V_{REFDAC} = 1.024V, External Reference Mode $V_{REFDAC} = V_{REFIN}$)

DIFFERENTIAL OUTPUT VOLTAGE	OFFSET BINARY (DD0–DD9)	INPUT DECIMAL CODE
$\frac{V_{REFDAC}}{2.56} \times \frac{1023}{1023}$	11 1111 1111	1023
$\frac{V_{REFDAC}}{2.56} \times \frac{1021}{1023}$	11 1111 1110	1022
$\frac{V_{REFDAC}}{2.56} \times \frac{3}{1023}$	10 0000 0001	513
$\frac{V_{REFDAC}}{2.56} \times \frac{1}{1023}$	10 0000 0000	512
$\frac{-V_{REFDAC}}{2.56} \times \frac{1}{1023}$	01 1111 1111	511
$\frac{-V_{REFDAC}}{2.56} \times \frac{1021}{1023}$	00 0000 0001	1
$\frac{-V_{REFDAC}}{2.56} \times \frac{1023}{1023}$	00 0000 0000	0

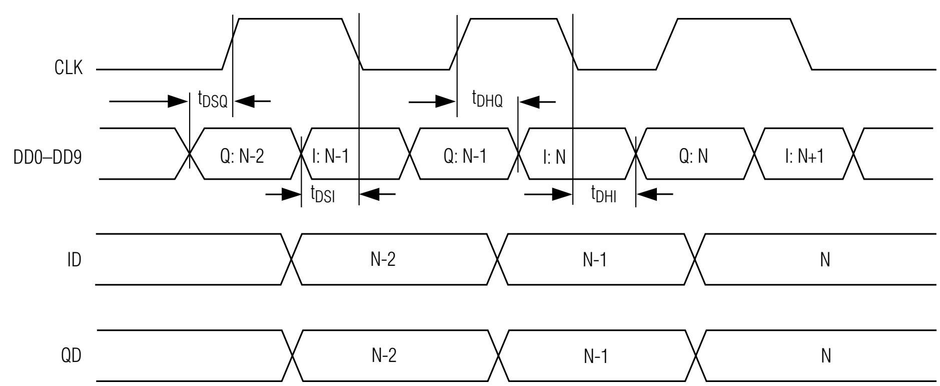


Figure 4. DAC System Timing Diagram

DAC Timing

Figure 4 shows the relationship between the clock, input data, and analog outputs. Data for the I channel (ID) is latched on the falling edge of the clock signal, and Q-channel (QD) data is latched on the rising edge of the clock signal. Both I and Q outputs are simultaneously updated on the next rising edge of the clock signal.

3-Wire Serial Interface and Operation Modes

The 3-wire serial interface controls the MAX5865 operation modes. Upon power-up, the MAX5865 must be programmed to operate in the desired mode. Use the 3-wire serial interface to program the device for the shutdown, idle, standby, Rx, Tx, or Xcvr mode. An 8-bit data register sets the operation modes as shown in Table 3. The serial interface remains active in all six modes.

Table 3. MAX5865 Operation Modes

FUNCTION	DESCRIPTION	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0
Shutdown	Device shutdown. REF is off, ADCs are off, and the ADC bus is tri-stated; DACs are off and the DAC input bus must be set to zero or OV_{DD}.	X	X	X	X	X	0	0	0
Idle	REF and CLK are on, ADCs are off, and the ADC bus is tri-stated; DACs are off and the DAC input bus must be set to zero or OV_{DD}.	X	X	X	X	X	0	0	1
Rx	REF is on, ADCs are on; DACs are off, and the DAC input bus must be set to zero or OV_{DD}.	X	X	X	X	X	0	1	0
Tx	REF is on, ADCs are off, and the ADC bus is tri-stated; DACs are on.	X	X	X	X	X	0	1	1
Xcvr	REF is on, ADCs and DACs are on.	X	X	X	X	X	1	0	0
Standby	REF is on, ADCs are off, and the ADC bus is tri-stated; DACs are off and the DAC input bus must be set to zero or OV_{DD}.	X	X	X	X	X	1	0	1

X = *Don't care.*

Shutdown mode offers the most dramatic power savings by shutting down all the analog sections of the MAX5865 and placing the ADCs' digital outputs in tri-state mode. When the ADCs' outputs transition from tri-state to on, the last converted word is placed on the digital outputs. The DACs' digital bus inputs must be zero or OV_{DD} because the bus is not internally pulled up. The DACs' previously stored data is lost when coming out of shutdown mode. The wake-up time from shutdown mode is dominated by the time required to charge the capacitors at REFP, REFN, and COM. In internal reference mode and buffered external reference mode, the wake-up time is typically 40µs to enter Xcvr mode, 20µs to enter Rx mode, and 40µs to enter Tx MODE.

In idle mode, the reference and clock distribution circuits are powered, but all other functions are off. The ADCs' outputs are forced to tri-state. The DACs' digital bus inputs must be zero or OV_{DD}, because the bus is not internally pulled up. The wake-up time from the idle mode is 10µs required for the ADCs and DACs to be fully operational. When the ADCs' outputs transition from tri-state to on, the last converted word is placed on the digital outputs. In the idle mode, the supply current is lowered if the clock input is set to zero or OV_{DD}; however, the wake-up time extends to 40µs.

In standby mode, only the ADCs' reference is powered; the rest of the device's functions are off. The pipeline ADCs are off and DA0 to DA7 are in tri-state mode. The DACs' digital bus inputs must be zero or OV_{DD} because the bus is not internally pulled up. The wake-up time from standby mode to the Xcvr mode is dominated by the 40µs required to activate the pipeline ADCs and DACs. When the ADC outputs transition from tri-state to active, the last converted word is placed on the digital outputs.

The serial digital interface is a standard 3-wire connection compatible with SPI/QSPI™/MICROWIRE/DSP interfaces. Set $\overline{CS}$ low to enable the serial data loading at DIN. Following $\overline{CS}$ high-to-low transition, data is shifted synchronously, MSB first, on the rising edge of the serial clock (SCLK). After 8 bits are loaded into the serial input register, data is transferred to the latch. $\overline{CS}$ must transition high for a minimum of 80ns before the next write sequence. The SCLK can idle either high or low between transitions. Figure 5 shows the detailed timing diagram of the 3-wire serial interface.

QSPI is a trademark of Motorola, Inc.

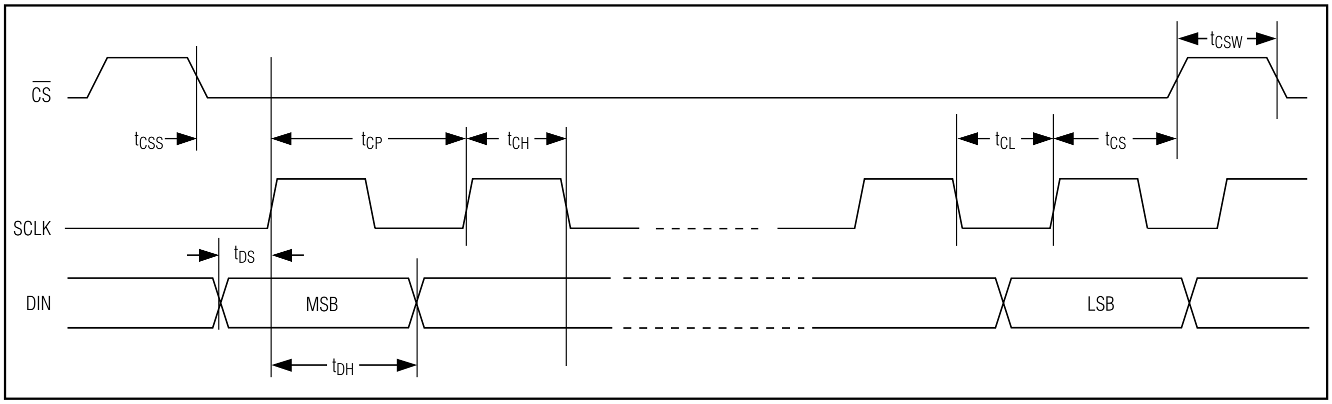


Figure 5. 3-Wire Serial Interface Timing Diagram

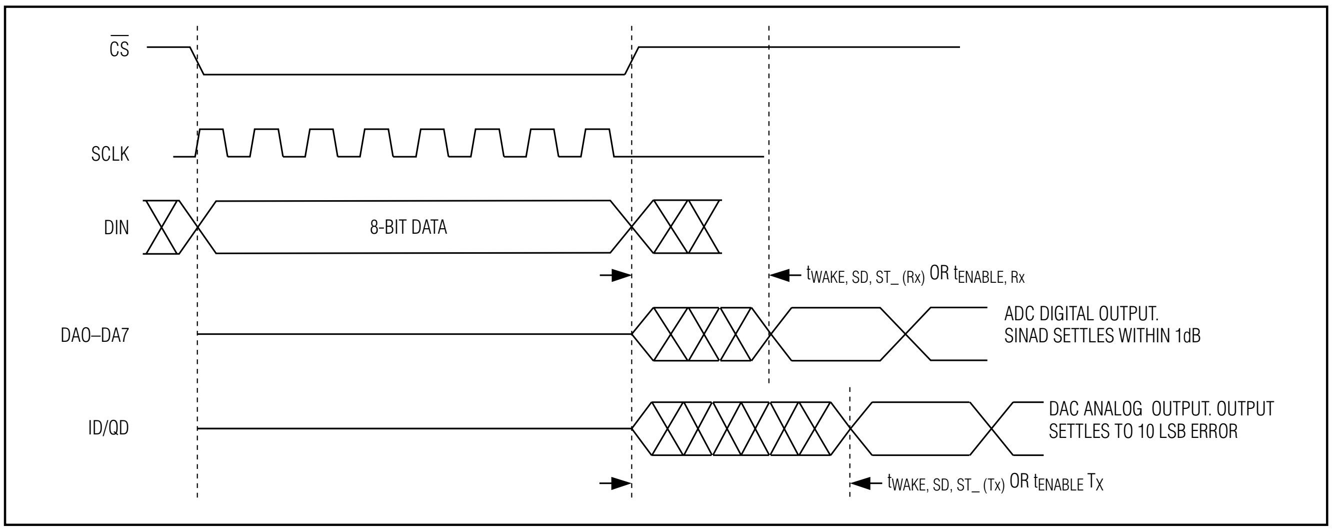


Figure 6. MAX5865 Mode Recovery Timing Diagram

Mode Recovery Timing

Figure 6 shows the mode recovery timing diagram. t_{WAKE} is the wake-up time when exiting shutdown, idle, or standby mode and entering into Rx, Tx, or Xcvr mode. t_{ENABLE} is the recovery time when switching between any Rx, Tx, or Xcvr mode. t_{WAKE} or t_{ENABLE} is the time for the ADC to settle within 1dB of specified SINAD performance and DAC settling to 10 LSB error. t_{WAKE} or t_{ENABLE} times are measured after the 8-bit serial command is latched into the MAX5865 by $\overline{CS}$ transition high. t_{ENABLE} for Xcvr mode is dominated by the DAC wake-up time. The recovery time is 10µs to switch between Xcvr, Tx, or Rx modes. The recovery time is 40µs to switch from shutdown or standby mode to Xcvr mode.

System Clock Input (CLK)

CLK input is shared by both the ADCs and DACs. It accepts a CMOS-compatible signal level set by OV_{DD} from 1.8V to V_{DD}. Since the interstage conversion of the device depends on the repeatability of the rising and falling edges of the external clock, use a clock with low jitter and fast rise and fall times (<2ns). Specifically, sampling occurs on the rising edge of the clock signal, requiring this edge to provide the lowest possible jitter. Any significant clock jitter limits the SNR performance of the on-chip ADCs as follows:

$$SNR = 20 \times \log\left(\frac{1}{2 \times \pi \times t_{IN} \times t_{AJ}}\right)$$

where f_{IN} represents the analog input frequency and t_{AJ} is the time of the clock jitter.

Clock jitter is especially critical for undersampling applications. Consider the clock input as an analog input and route away from any analog input or other digital signal lines. The MAX5865 clock input operates with an $OV_{DD}/2$ voltage threshold and accepts a 50% ±15% duty cycle.

Reference Configurations

The MAX5865 features an internal precision 1.024V bandgap reference that is stable over the entire power supply and temperature range. The REFIN input provides two modes of reference operation. The voltage at REFIN (V_{REFIN}) sets reference operation mode (Table 4).

In internal reference mode, connect REFIN to V_{DD}. V_{REF} is an internally generated 0.512V. COM, REFP, and REFN are low-impedance outputs with $V_{COM} = V_{DD}/2$, $V_{REFP} = V_{DD}/2 + V_{REF}/2$, and $V_{REFN} = V_{DD}/2 - V_{REF}/2$. Bypass REFP, REFN, and COM each with a 0.33µF capacitor. Bypass REFIN to GND with a 0.1µF capacitor.

In buffered external reference mode, apply 1.024V ±10% at REFIN. In this mode, COM, REFP, and REFN are low-impedance outputs with $V_{COM} = V_{DD}/2$, $V_{REFP} = V_{DD}/2 + V_{REFIN}/4$, and $V_{REFN} = V_{DD}/2 - V_{REFIN}/4$. Bypass REFP, REFN, and COM each with a 0.33µF capacitor. Bypass REFIN to GND with a 0.1µF capacitor. In this mode, the DAC's full-scale output voltage and common-mode voltage are proportional to the external reference. For example, if the V_{REFIN} is increased by 10% (max), the DACs' full-scale output voltage is also increased by 10% or to ±440mV, and the common-mode voltage increases by 10%.

Table 4. Reference Modes

V_{REFIN}	REFERENCE MODE
>0. 8 x V_{DD}	Internal reference mode. V_{REF} is internally generated to be 0.512V. Bypass REFP, REFN, and COM each with a 0.33µF capacitor.
1.024V ±10%	Buffered external reference mode. An external 1.024V ±10% reference voltage is applied to REFIN. V_{REF} is internally generated to be $V_{REFIN}/2$. Bypass REFP, REFN, and COM each with a 0.33µF capacitor. Bypass REFIN to GND with a 0.1µF capacitor.

Applications Information

Using Balun Transformer AC-Coupling

An RF transformer (Figure 7) provides an excellent solution to convert a single-ended signal source to a fully differential signal for optimum ADC performance. Connecting the center tap of the transformer to COM provides a $V_{DD}/2$ DC level shift to the input. A 1:1 transformer can be used, or a step-up transformer can be selected to reduce the drive requirements. In general, the MAX5865 provides better SFDR and THD with fully differential input signals than single-ended signals, especially for high-input frequencies. In differential mode, even-order harmonics are lower as both inputs (IA+, IA-, QA+, QA-) are balanced, and each of the ADC inputs only requires half the signal swing compared to single-ended mode. Figure 8 shows an RF transformer converting the MAX5865 DACs' differential analog outputs to single ended.

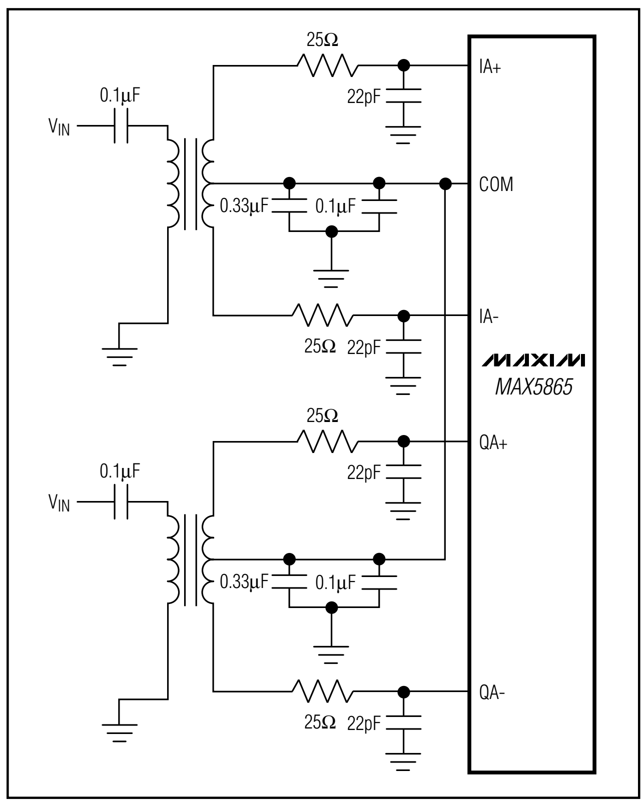


Figure 7. Balun-Transformer Coupled Single-Ended to Differential Input Drive for ADCs

Ultra-Low-Power, High-Dynamic-Performance, 40Msps Analog Front End

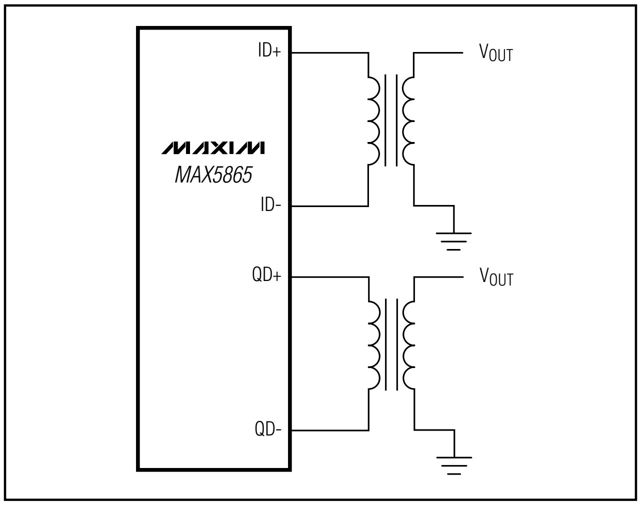


Figure 8. Balun-Transformer Coupled Differential to Single-Ended Output Drive for DACs

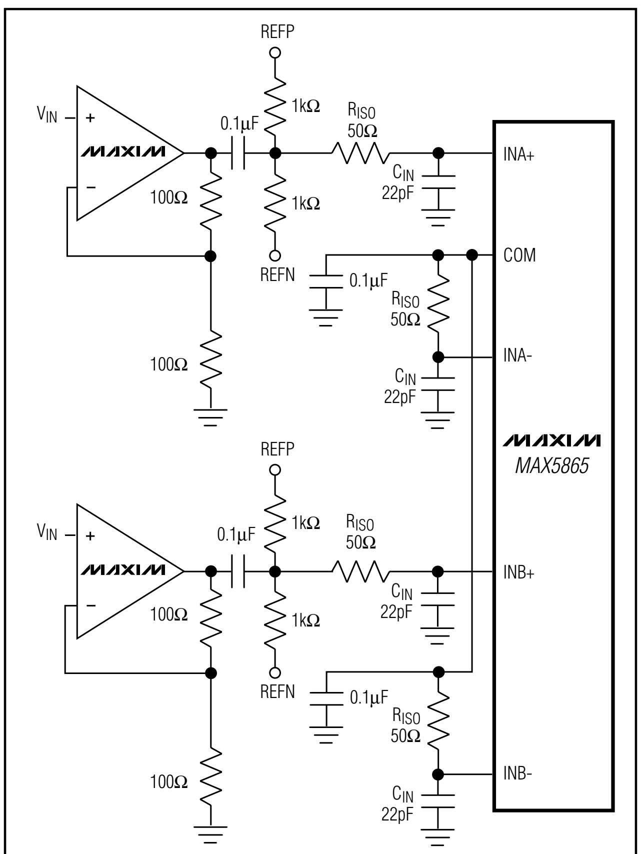


Figure 9. Single-Ended Drive for ADCs

Using Op-Amp Coupling

Drive the MAX5865 ADCs with op amps when a balun transformer is not available. Figures 9 and 10 show the ADCs being driven by op amps for AC-coupled single-ended, and DC-coupled differential applications. Amplifiers such as the MAX4354/MAX4454 provide high speed, high bandwidth, low noise, and low distortion to maintain the input signal integrity. Figure 10 can also be used to interface with the DAC differential analog outputs to provide gain or buffering. The DAC differential analog outputs cannot be used in single-ended mode because of the internally generated 1.4VDC common-mode level. Also, the DAC analog outputs are designed to drive a differential input stage with input impedance ≥70kΩ. If single-ended outputs are desired, use an amplifier to provide differential to single-ended conversion and select an amplifier with proper input common-mode voltage range.

FDD and TDD Modes

The MAX5865 can be used in diverse applications operating FDD or TDD modes. The MAX5865 operates in Xcvr mode for FDD applications such as WCDMA-3GPP (FDD) and 4G technologies. Also, the MAX5865 can switch between Tx and Rx modes for TDD applications like TD-SCDMA, WCDMA-3GPP (TDD), IEEE802.11a/b/g, and IEEE802.16.

In FDD mode, the ADC and DAC operate simultaneously. The ADC bus and DAC bus are dedicated and must be connected in 18-bit parallel (8-bit ADC and 10-bit DAC) to the digital baseband processor. Select Xcvr mode through the 3-wire serial interface and use the conversion clock to latch data. In FDD mode, the MAX5865 uses 75.6mW power at f_{CLK} = 40MHz. This is the total power of the ADC and DAC operating simultaneously.

In TDD mode, the ADC and DAC operate independently. The ADC and DAC bus are shared and can be connected together, forming a single 10-bit parallel bus to the digital baseband processor. Using the 3-wire serial interface, select between Rx mode to enable the ADC and Tx mode to enable the DAC. When operating in Rx mode, the DAC does not transmit because the core is disabled and in Tx mode, the ADC bus is tri-state. This eliminates any unwanted spurious emissions and prevents bus contention. In TDD mode, the MAX5865 uses 63mW power in Rx mode at f_{CLK} = 40MHz, and the DAC uses 38.4mW in Tx mode.

Figure 11 illustrates the MAX5865 working with the MAX2820 in TDD mode to provide a complete 802.11b radio front-end solution. Because the MAX5865 DAC has full differential analog outputs with a common-mode level of 1.4V, and the ADC has wide-input common-mode

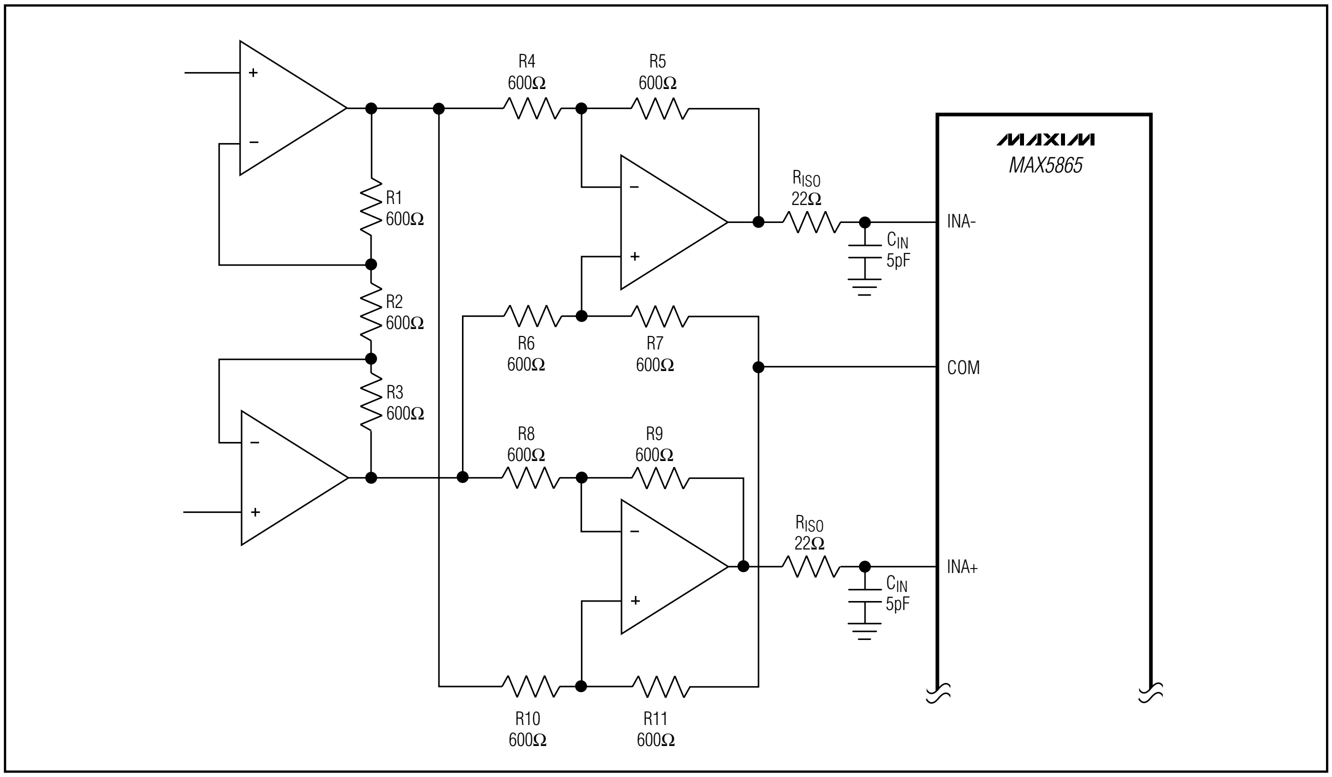


Figure 10. ADC DC-Coupled Differential Drive

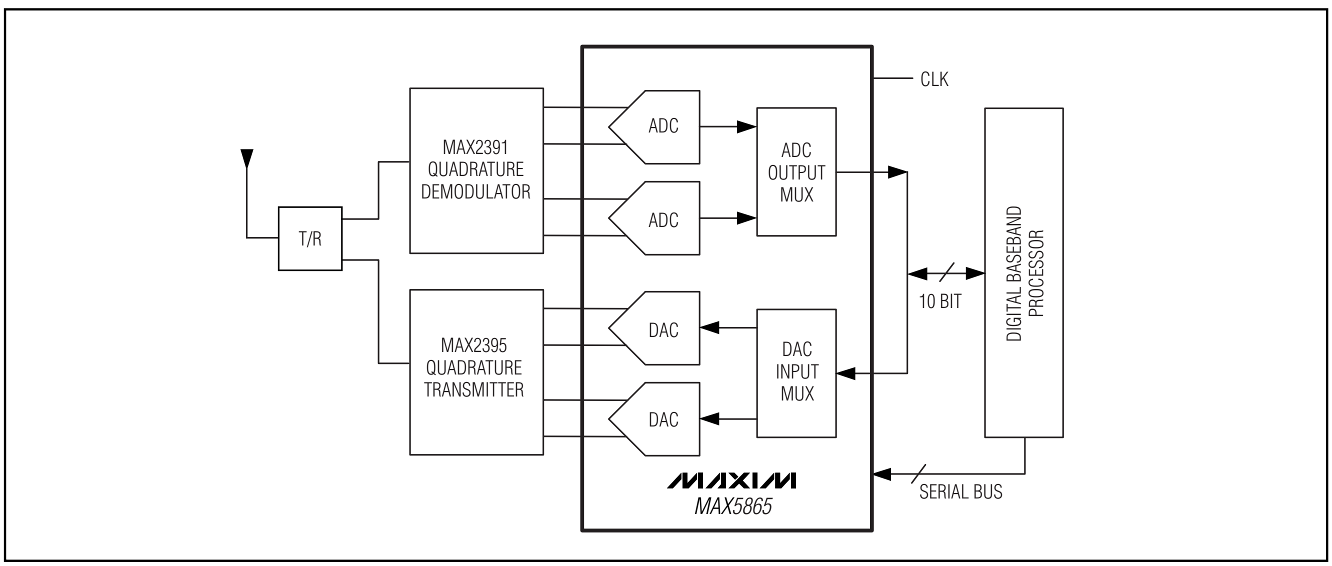


Figure 11. Typical Application Circuit for TDD

range, it can interface directly with RF transceivers while eliminating discrete components and amplifiers used for level-shifting circuits. Also, the DAC's full dynamic range is preserved because the internally generated common-mode level eliminates code-generated level shifting or attenuation due to resistor level shifting. The MAX5865 ADC has $1V_{P-P}$ full-scale range and accepts input common-mode levels of $V_{DD}/2$ (±200mV). These features simplify the analog interface between RF quadrature demodulator and ADC while eliminating discrete gain amplifiers and level-shifting components.

Grounding, Bypassing, and Board Layout

The MAX5865 requires high-speed board layout design techniques. Refer to the MAX5865 EV kit data sheet for a board layout reference. Locate all bypass capacitors as close to the device as possible, preferably on the same side of the board as the device, using surface-mount devices for minimum inductance. Bypass V_{DD} to GND with a 0.1µF ceramic capacitor in parallel with a 2.2µF capacitor. Bypass OV_{DD} to OGND with a 0.1µF ceramic capacitor in parallel with a 2.2µF capacitor. Bypass REFP, REFN, and COM each to GND with a 0.33µF ceramic capacitor. Bypass REFIN to GND with a 0.1µF capacitor.

Multilayer boards with separated ground and power planes yield the highest level of signal integrity. Use a split ground plane arranged to match the physical location of the analog ground (GND) and the digital output driver ground (OGND) on the device package. Connect the MAX5865 exposed backside paddle to the GND plane. Join the two ground planes at a single point such that the noisy digital ground currents do not interfere with the analog ground plane. The ideal location for this connection can be determined experimentally at a point along the gap between the two ground planes. Make this connection with a low-value, surface-mount resistor (1Ω to 5Ω), a ferrite bead, or a direct short. Alternatively, all ground pins could share the same ground plane, if the ground plane is sufficiently isolated from any noisy digital system's ground plane (e.g., downstream output buffer or DSP ground plane).

Route high-speed digital signal traces away from sensitive analog traces. Make sure to isolate the analog input lines to each respective converter to minimize channel-to-channel crosstalk. Keep all signal lines short and free of 90° turns.

Dynamic Parameter Definitions

ADC and DAC Static Parameter Definitions

Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. The static linearity parameters for the device are measured using the end-point method. (DAC Figure 12a).

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees no missing codes (ADC) and a monotonic transfer function (ADC and DAC) (DAC Figure 12b).

ADC Offset Error

Ideally, the midscale transition occurs at 0.5 LSB above midscale. The offset error is the amount of deviation between the measured transition point and the ideal transition point.

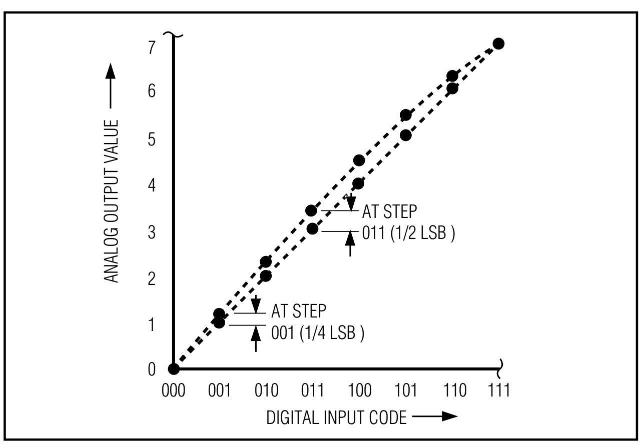


Figure 12a. Integral Nonlinearity

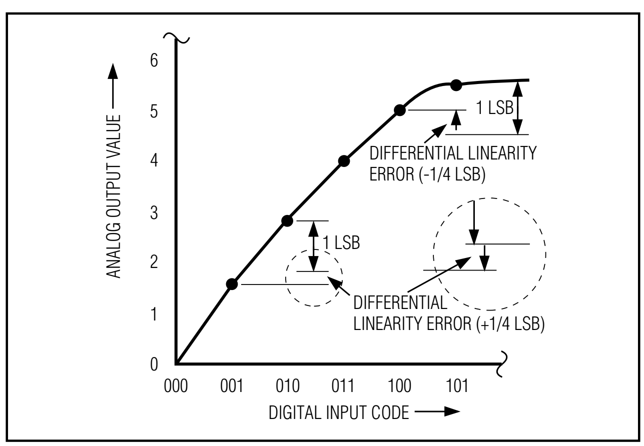


Figure 12b. Differential Nonlinearity

DAC Offset Error

Offset error (Figure 12a) is the difference between the ideal and actual offset point. The offset point is the output value when the digital input is midscale. This error affects all codes by the same amount and usually can be compensated by trimming.

ADC Gain Error

Ideally, the ADC full-scale transition occurs at 1.5 LSB below full scale. The gain error is the amount of deviation between the measured transition point and the ideal transition point with the offset error removed.

ADC Dynamic Parameter Definitions

Aperture Jitter

Figure 13 depicts the aperture jitter (t_{AJ}), which is the sample-to-sample variation in the aperture delay.

Aperture Delay

Aperture delay (t_{AD}) is the time defined between the rising edge of the sampling clock and the instant when an actual sample is taken (Figure 13).

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error) and results directly from the ADC's resolution (N bits):

$$SNR(max) = 6.02dB \times N + 1.76dB \text{ (in dB)}$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise. RMS noise includes all spectral components to the Nyquist frequency excluding the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion (SINAD)

SINAD is computed by taking the ratio of the RMS signal to the RMS noise. RMS noise includes all spectral components to the Nyquist frequency excluding the fundamental and the DC offset.

Effective Number of Bits (ENOB)

ENOB specifies the dynamic performance of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. ENOB for a full-scale sinusoidal input waveform is computed from:

$$ENOB = (SINAD - 1.76) / 6.02$$

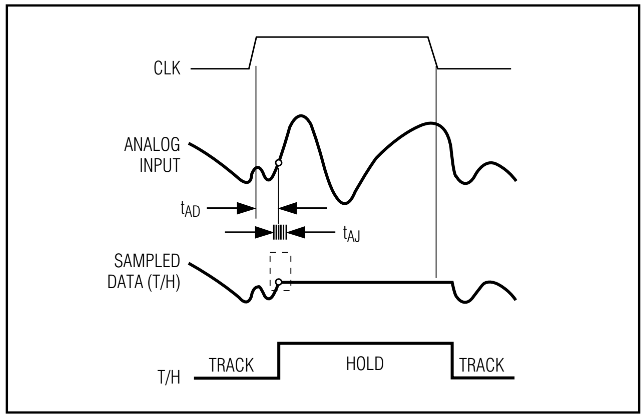


Figure 13. T/H Aperture Timing

Total Harmonic Distortion (THD)

THD is typically the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20\log\left[\frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2)}}{V_1}\right]$$

where V_1 is the fundamental amplitude and V_2–V_6 are the amplitudes of the 2nd- through 6th-order harmonics.

Third Harmonic Distortion (HD3)

HD3 is defined as the ratio of the RMS value of the third harmonic component to the fundamental input signal.

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio expressed in decibels of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest spurious component, excluding DC offset.

Intermodulation Distortion (IMD)

IMD is the total power of the intermodulation products relative to the total input power when two tones, f_1 and f_2, are present at the inputs. The intermodulation products are ($f_1 \pm f_2$), ($2 \times f_1$), ($2 \times f_2$), ($2 \times f_1 \pm f_2$), ($2 \times f_2 \pm f_1$). The individual input tone levels are at -7dBFS.

3rd-Order Intermodulation (IM3)

IM3 is the power of the worst third-order intermodulation product relative to the input power of either input tone when two tones, f_1 and f_2, are present at the inputs. The 3rd-order intermodulation products are ($2 \times f_1 \pm f_2$), ($2 \times f_2 \pm f_1$). The individual input tone levels are at -7dBFS.

Power-Supply Rejection

Power-supply rejection is defined as the shift in offset and gain error when the power supply is changed ±5%.

Small-Signal Bandwidth

A small -20dBFS analog input signal is applied to an ADC in such a way that the signal's slew rate does not limit the ADC's performance. The input frequency is then swept up to the point where the amplitude of the digitized conversion result has decreased by 3dB. Note that the T/H performance is usually the limiting factor for the small-signal input bandwidth.

Full-Power Bandwidth

A large -0.5dBFS analog input signal is applied to an ADC, and the input frequency is swept up to the point where the amplitude of the digitized conversion result has decreased by 3dB. This point is defined as the full-power bandwidth frequency.

DAC Dynamic Parameter Definitions

Total Harmonic Distortion

THD is the ratio of the RMS sum of the output harmonics up to the Nyquist frequency divided by the fundamental:

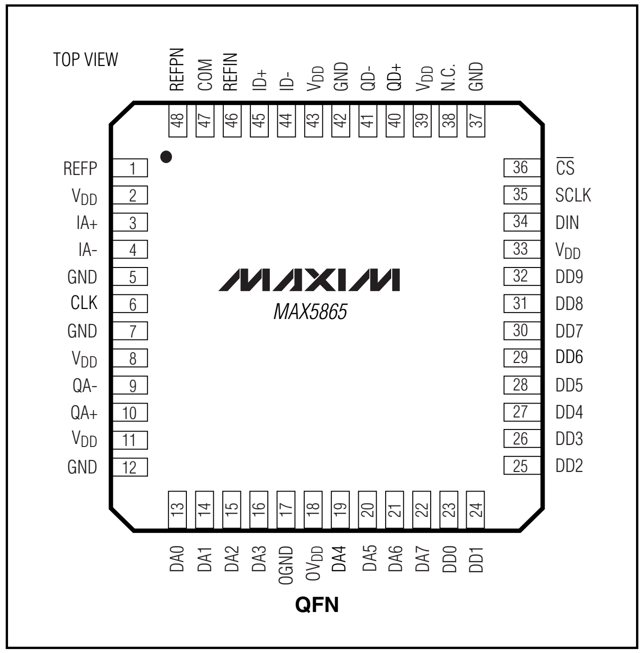
$$THD = 20\log\left[\frac{\sqrt{(V_2^2 + V_3^2 + \ldots + V_n^2)}}{V_1}\right]$$

where V_1 is the fundamental amplitude and V_2 through V_n are the amplitudes of the 2nd through nth harmonic up to the Nyquist frequency.

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest distortion component up to the Nyquist frequency excluding DC.

Pin Configuration



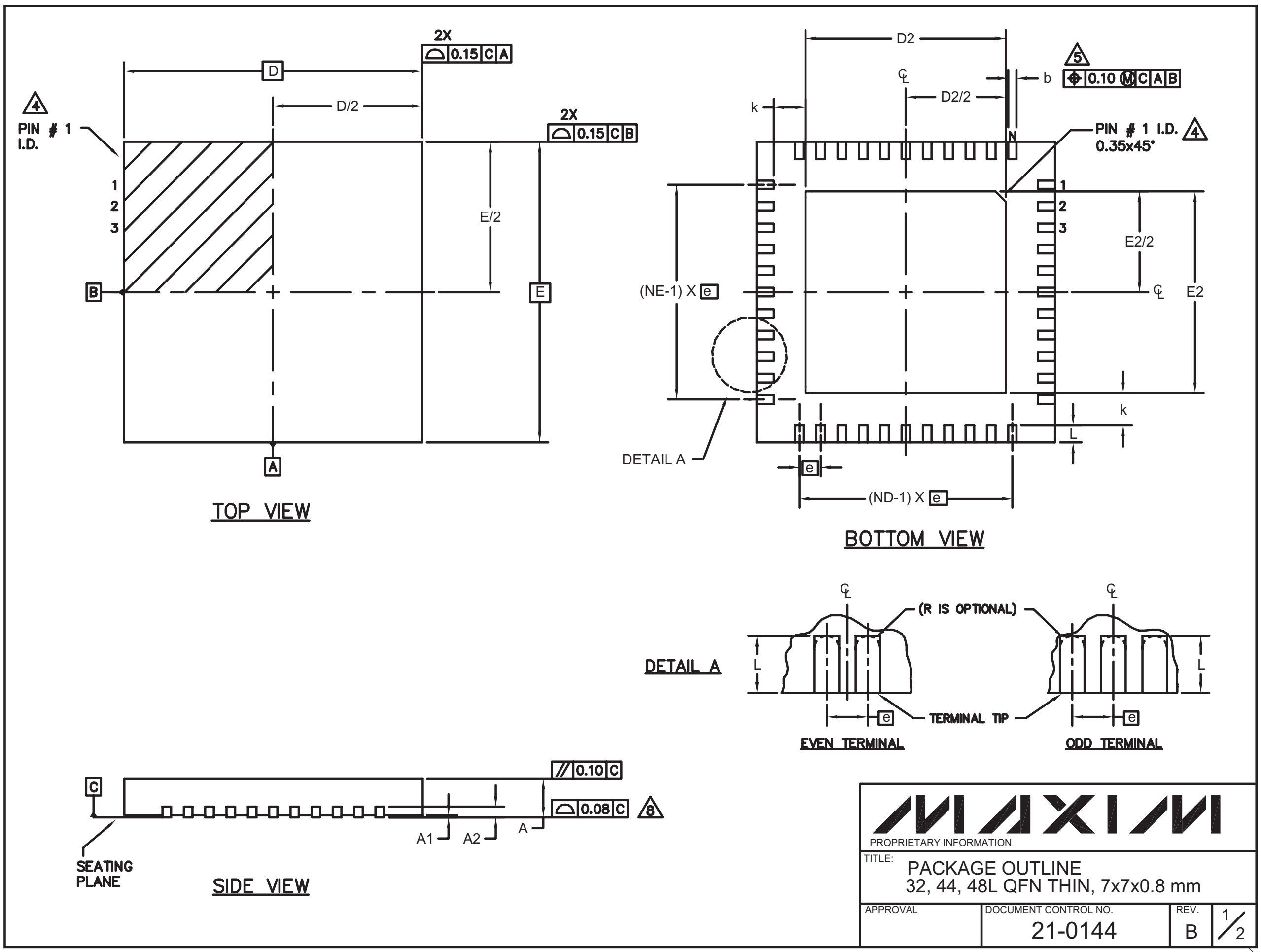
Chip Information

TRANSISTOR COUNT: 16,765

PROCESS: CMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Ultra-Low-Power, High-Dynamic-Performance, 40Msps Analog Front End

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS

PKG	32L 7x7			44L 7x7			48L 7x7			CUSTOM PKG. (T4877-1) 48L 7x7		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.20	0.25	0.30
D	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
E	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.45	0.55	0.65
N	32			44			48			44		
ND	8			11			12			10		
NE	8			11			12			12		

EXPOSED PAD VARIATIONS

PKG. CODES	DEPOPULATED LEADS	D2			E2			JEDEC MO220 REV. C
		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T3277-1	-	4.55	4.70	4.85	4.55	4.70	4.85	-
T4477-1	-	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1
T4877-1**	13, 24, 37, 48	4.20	4.30	4.40	4.20	4.30	4.40	-
T4877-2	-	5.45	5.60	5.63	5.45	5.60	5.63	WKKD-2

** NOTE: T4877-1 IS A CUSTOM 48L PKG. WITH 4 LEADS DEPOPULATED. TOTAL NUMBER OF LEADS ARE 44.

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M−1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95−1 SPP−012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE
32, 44, 48L QFN THIN, 7x7x0.8 mm

APPROVAL | DOCUMENT CONTROL NO. 21-0144 | REV. B | 2/2

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